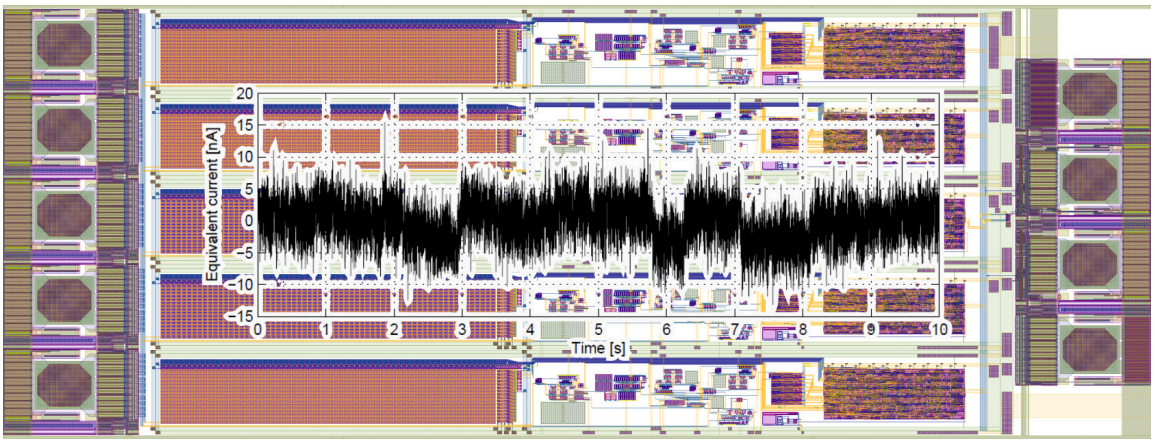
Centre Nacional de Microelectrònica IMB

CSIC
Consejo Superior de Investigaciones Científicas

Master Thesis
at the Integrated Circuits and Systems (ICAS) research group of IMB-CNM(CSIC)

Design of a CMOS Random Telegraph Noise Test Chip

Description



Analog and mixed-signal CMOS circuits for low-frequency sensing applications suffer from random telegraph noise (RTN) as one of the major limiting factors when scaling their area and power. Unfortunately, semiconductor foundries lack of RTN models for circuit simulation. This work aims to design an application-specific integrated circuit (ASIC) in 180-nm CMOS technology containing thousands of transistors to characterize their RTN. For this purpose, the ASIC will also integrate the transistor selection logic, a low-noise integrate-and-fire (IAF) ADC and a standard I^2C digital interface.

Background and skills

- Electronic engineering or any similar curriculum covering the following topics: CMOS technology basics, photodiode devices, analog and mixed-signal CMOS circuit design.
- Knowledge of EDA tools and HDLs for full-custom IC design.
- Capability of working as a team.
- Good spoken and written English.

Tasks

The student will design the analog and mixed-signal parts of the ASIC in a given 180-nm 1.8-V CMOS technology following the full-custom IC design methodology through Cadence EDA tools. Apart from low-noise operation and compact circuit area, the design will be optimized for its robustness against process-supply-temperature (PVT) variations. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

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