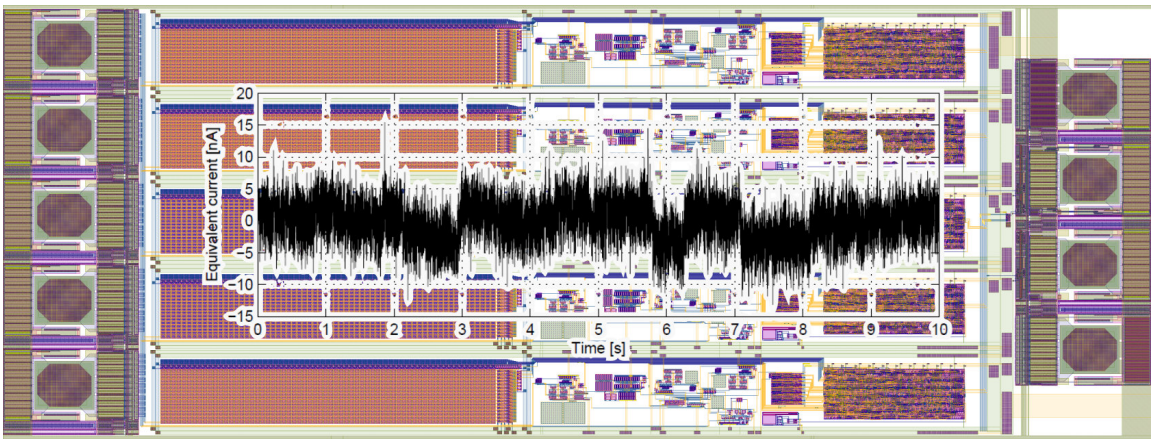
Centre Nacional de Microelectrònica IMB

CSIC
Consejo Superior de Investigaciones Científicas

**Bachelor Thesis**
at the Integrated Circuits and Systems (ICAS) research group of IMB-CNM(CSIC)

# Characterization of a CMOS Random Telegraph Noise Test Chip

## Description




Analog and mixed-signal CMOS circuits for low-frequency sensing applications suffer from random telegraph noise (RTN) as one of the major limiting factors when scaling their area and power. Unfortunately, semiconductor foundries lack of RTN models for circuit simulation. This work aims to test an application-specific integrated circuit (ASIC) designed at IMB-CNM and fabricated in 180-nm CMOS technology, which contains thousands of transistors to characterize their RTN. For this purpose, the ASIC also integrates the transistor selection logic, low-noise IAF ADCs and a standard $I^2C$ interface.

## Background and skills

- Electronic engineering or any similar curriculum covering the following topics: analog circuit design, FPGA-based platforms, instrumentation, data processing.
- Knowledge of FPGA kits and lab virtualization tools.
- Experience in Python programming language.
- Capability of working as a team.
- Good spoken and written English.

## Tasks

The student will develop the laboratory setup to automate the characterization of the RTN test chips. This measurement environment will include the custom chip carrier PCB, a standard FPGA-based interface as the hardware bridge between the ASIC and the PC, a well as available laboratory instrumentation. The FPGA will be also in charge of controlling the rest of laboratory instruments. In this sense, the overall instrument virtualization will be implemented with a Python user interface. The developed setup will be validated through the test of one or more RTN ASIC units. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

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