Ion implantation facilities

Processes performed at Ion implantation facilities

Techniques

Ion implantation technology is a process technique in semiconductors industry for surface doping which presents multiple advantages such as:

- Precise control on doping depth profile.
- Low temperature process, i. e. compatible with photoresist mask.
- Wide selection of masking materials: photoresist, oxide, poly-Si, metal…
- Lateral doping uniformity.

Two **medium-current ion implanters** are available at IMB-CNM to implant different atomic species: B, P, As, N, Al, Si, Mg, O, He...

Equipment

a) Ion Implanter IMC 210RD:

- Liquid, gas and solid sources.
- Available precursors: BF_3, SiF_4, N_2, Ar, CO_2, He/Ar, As, P, Mg, $AlCl_3$, GeS_2 and H_2O.
- Implanted doses from 1.0×10^{11} at/cm^2 to 5.0×10^{15} at/cm^2.
- Energy range: from 3 keV to 210 keV (single charge).
- Equipped with two processing chambers: standard (ES) and research and development (RD) chambers.
- ES chamber: Automated loading system.
- RD chamber: Manual loading system. Possibility to process thin wafer (thickness<400 µm) and small pieces. Holder allows to heat wafers up to 500ºC.
- Tilt range: From 0° to 15° and from 0° to 10° at ES chamber and RD chamber, respectively.
- Maximum wafer size: 4 inch wafers and 6 inch wafers for ES and RD chamber, respectively.
- Temperature: Possibility to heat wafer up to 500 °C.

- Exclusively to process CMOS samples.

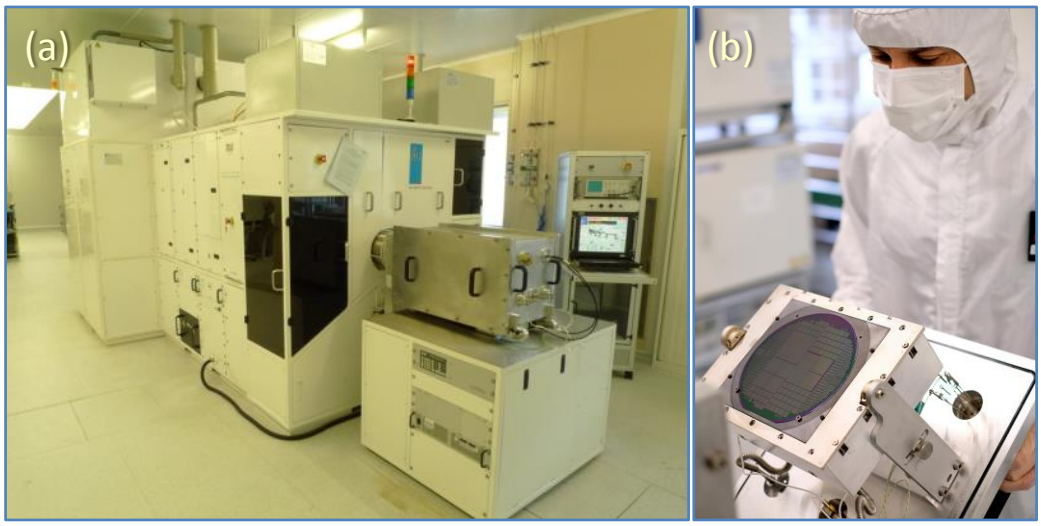

Fig. 1: (a) Picture of the ion implanter IMC210 at the clean room of the IMB-CNM and (b) detail of the sampleholder of the RD chamber.

b) Ion Implanter EATON NV4206:

- Available precursors: BF_3, SiF_4, Ar, N_2, and P.
- Gas and solid sources.
- Implanted doses from 1.0×10^{12} at/cm^2 to 5.0×10^{15} at/cm^2.
- Energy range: 30 keV to150 keV (single charge).
- Tilt range: From 1° to 15° value. Dose measurement limited to 7° via software.
- Maximum wafer size: 4 inch wafers.
- Exclusively to process CMOS samples.

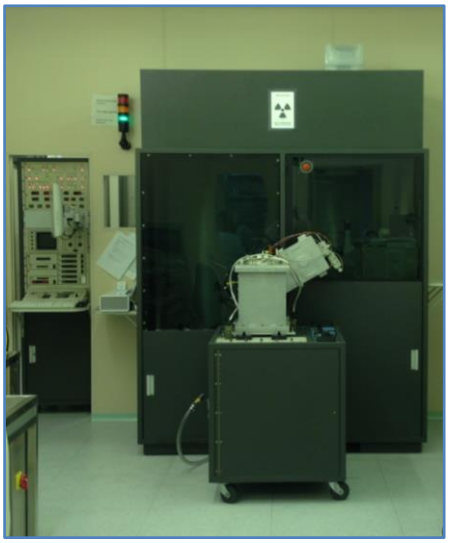

Fig. 2: Ion implantation system EATON NV4026.

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