Centre Nacional de Microelectrònica IMB

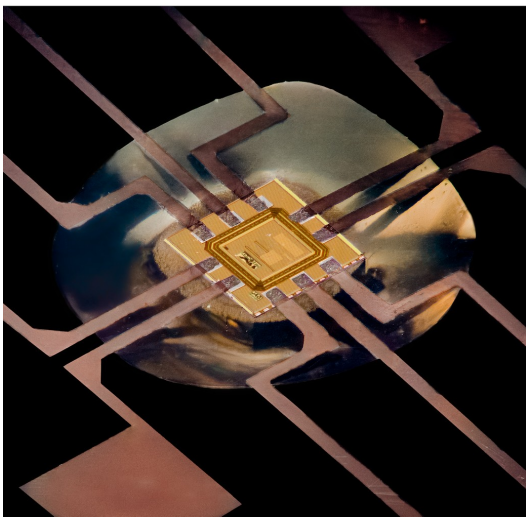
CSIC
Consejo Superior de Investigaciones Científicas

Treball Final de Grau

Experimental Characterization of a Smart ISFET CMOS Chip

Description

This work aims to test an application-specific integrated circuit (ASIC) designed at IMB-CNM(CSIC) and fabricated in CMOS technology, which contains several ion-sensitive field-effect transistors (ISFETs) as electrochemical sensors. Indeed, each ISFET cell integrated in the chip includes a novel CMOS A/D converter circuit for the biasing, configuration, compensation and A/D conversion of its own potentiometric measurements. The experimental characterization of this smart ISFETs at electrical and electrochemical levels requires of a custom FPGA-based hardware and a Python software user interface.



Background and skills

- Electronic engineering or any similar curriculum covering the following topics: analog circuit design, FPGA-based platforms, instrumentation, data processing.
- Knowledge of FPGA kits and lab virtualization tools.
- Experience in Python programming language.
- Capability of working as a team.
- Good spoken and written English.

Tasks

The student will develop the laboratory setup to characterize the smart ISFET chip both at electrical and electrochemical levels. This measurement environment includes the chip carrier PCB, a standard or custom FPGA-based interface to be the hardware bridge for the digital communications between the ASIC and a PC. Such digital communications cover the configuration and calibration of the integrated circuit and the digital read-out of its electrochemical measurements. The virtualization of the equivalent instrument will be implemented with a Python user interface. The developed setup will be validated through the test of one or more ASIC units. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

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