Centre Nacional de Microelectrònica IMB

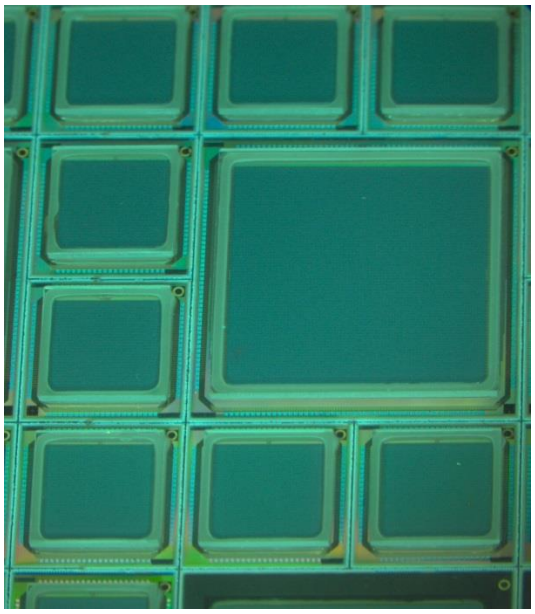
CSIC
CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

Master Thesis (with possibility of PhD Thesis)
at the Integrated Circuits and Systems (ICAS) research group of IMB-CNM(CSIC)

Read-Out Integrated Circuit for High-Speed Infrared Imagers

Description

This work aims to explore new ultra low-power and compact-pitch analog and mixed-signal CMOS circuit design techniques for monolithic high-speed MWIR imagers. These IC imagers are based on focal plane arrays of digital pixel sensor (DPS) cells. The optimization of the read-out IC will be done both at pixel circuit and imager architectural levels. The AMS circuits to be designed include the in-pixel A/D data converter, its digital interface and the local analog biasing, while maintaining a low-power budget and a reduced silicon area. The target MWIR sensing technologies are already available at IMB-CNM or supplied by external partners. Special attention will be paid to investigate low-latency asynchronous read-out strategies, like address-event representation (AER) protocols at the focal plane level.



Background and skills

- Electronic engineering or any similar curriculum covering the following topics: CMOS technology basics, MOS device modeling, analog and digital CMOS circuit design and A/D conversion architectures.
- Knowledge of EDA tools and HDLs for full-custom mixed-signal IC design.
- Capability of working as a team.
- Good spoken and written English.

Tasks

The student will design all the CMOS circuits of the digital pixel sensor IP following the standard full-custom mixed-signal IC design methodology including both schematic and layout. The target integration scaling will range from 180-nm to 65-nm CMOS technology nodes. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

Contact

Dr. Lluís Terés
lluis.teres@imb-cnm.csic.es

Dr. Francesc Serra Graells
paco.serra@imb-cnm.csic.es