Centre Nacional de Microelectrònica IMB

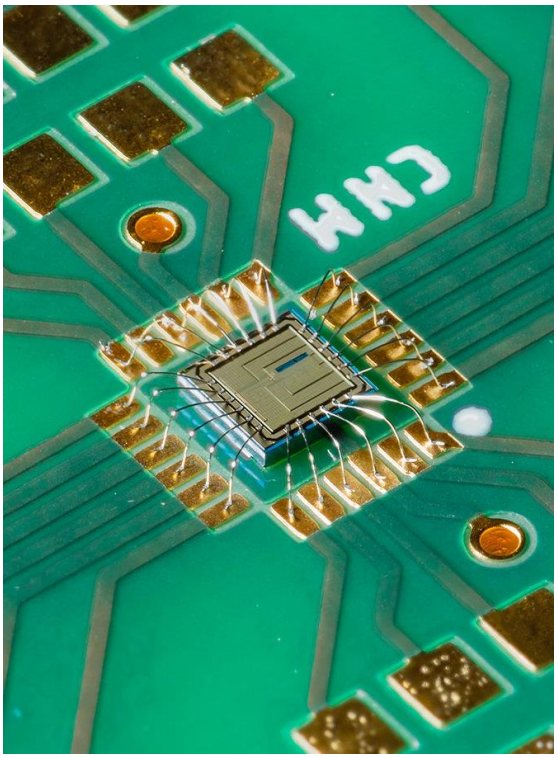
CSIC
Consejo Superior de Investigaciones Científicas

Master Thesis (with possibility of PhD Thesis)
at the Integrated Circuits and Systems (ICAS) research group of IMB-CNM(CSIC)

High-Resolution Audio A/D Data Converter IP Block in 22-nm CMOS Technology for RISC-V Systems-on-Chip

Description

The role of edge-of-the-cloud devices and the corresponding generation of big data are expected to include more than 10% of the world economy by 2030. In general, the massive deployment of ubiquitous smart sensing SoCs requires cost-effective power-efficient A/D converters (ADCs) capable of dealing with large dynamic range signals (typ. >80dB) but with practical bandwidth values not exceeding the kHz range in many applications. Oversampling Delta-Sigma (ΔΣ) modulators are well-suited ADC architectures for these scenarios. This work will design a 16-bit 20-kHz ΔΣ ADC circuit as a mixed-signal IP block in 22-nm 0.8-V CMOS technology. Design efforts will be focused not only on low-power operation and compact area, but also on technology/supply scalability. Furthermore, the ADC IP structure will ease its integration in a RISC-V SoC by including the analog preamplifier at the frontend, so commercial audio microphones can be employed, together with a digital decimator and AXI-4 Lite slave at its backend.



Background and skills

- Electronic engineering or any similar curriculum covering the following topics: CMOS technology basics, MOS device modeling, analog and digital CMOS circuit design and A/D conversion architectures.
- Knowledge of EDA tools and HDLs for full-custom and semi-custom IC design.
- Capability of working as a team.
- Good spoken and written English.

Tasks

The student will design the analog, mixed-signal and digital parts of the ΔΣ ADC IP circuit in a given 22-nm 0.8-V CMOS technology following the full-custom and semi-custom IC design methodologies through Cadence EDA tools. Apart from low-power operation and compact area, the schematic and layout design will be optimized for its robustness against process-supply-temperature (PVT) variations. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

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