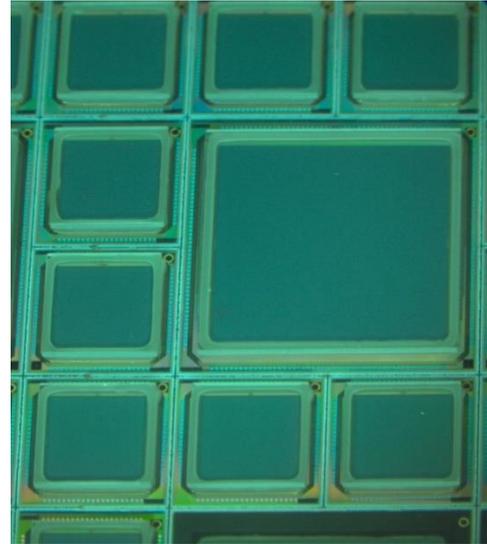

Job title **TFM: Read-Out Integrated Circuit for High-Speed Infrared Imagers**

Job description Master Thesis

Description

This work aims to explore new ultra low-power and compact-pitch analog and mixed-signal CMOS circuit design techniques for monolithic high-speed MWIR imagers. These IC imagers are based on focal plane arrays of digital pixel sensor (DPS) cells. The optimization of the read-out IC will be done both at pixel circuit and imager architectural levels. The AMS circuits to be design include the in-pixel A/D data converter, its digital interface and the local biasing, while maintaining a low-power budget and reduced silicon area. The target MWIR sensing technologies are already available at IMB-CNM or supplied by external partners. Special attention will be paid to investigate asynchronous read-out strategies, like address-event representation (AER) protocols.



Ideally, this Master Thesis should be the first step towards PhD studies addressing new families of IR imagers based on new architectures using AER read-out IC strategies.

Background and Skills

- Electronic engineering or any similar curriculum covering the following topics: CMOS technology basics, MOS device modeling, analog circuit theory, analog and digital CMOS circuit design, A/D conversion architectures and mixed signal processing.
- Knowledge of EDA tools and languages for full-custom ASIC design.
- Capability of working as a team.
- Good spoken and written English.

Tasks

The student will design all the CMOS circuits of the digital pixel sensor IP following the standard full-custom analog and mixed-signal (AMS) IC design methodology including both schematic and layout. The target integration scale will range from 180-nm to 65-nm CMOS technology nodes. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

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How to apply

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- This offer can be found on: <https://www.imb-cnm.csic.es/en/about-center/careers/open-positions>
- More information on IMB-CNM: <https://www.imb-cnm.csic.es/en/>

