





Institute of Microelectronics of Barcelona IMB-CNM (CSIC) C/- dels Til·lers, S.N., Campus UAB | 08193, Cerdanyola del Vallès <u>https://www.imb-cnm.csic.es</u> | <u>rrhh@imb-cnm.csic.es</u> +34 93 594 7700

Job title

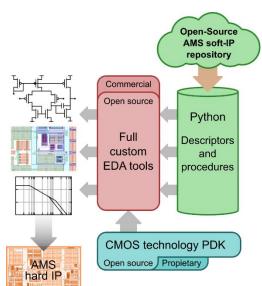
TFM: Open-Source Design Methodology for AMS Integrated Circuits

Job description

Master Thesis

Descripction

This work aims to explore new design methodologies of analog and mixedsignal (AMS) CMOS circuits in order to build a truly open-source, license-free and technology-portable repository of IP blocks. The proposed full-custom AMS IC design methodology is based on a common Python frontend, so expert designers can describe in detail the circuit topologies, simulation methodologies, optimization rules at transistor level, as well as the physical design constrains of these soft-IP AMS blocks. The goal is that a third-party designer should be able to use this soft-IP repository to develop an optimum hard-IP implementation in a CMOS technology of choice using either open-source or proprietary EDA tools and process design kits (PDKs).



Ideally, this Master Thesis should be the first step towards PhD studies dealing with Open-source hardware and AMS IC design methodologies, a highly promising domain.

Background and Skills

- Electronic engineering or any similar curriculum covering the following topics: CMOS technology basics, full-custom analog and mixed-signal CMOS circuit design.
- Knowledge of EDA tools and HDLs for full-custom IC design.
- Experience in Python programming language.
- Capability of working as a team.
- Good spoken and written English.







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Tasks

The student will setup a Python interface for the description of AMS CMOS IP circuits, both at schematic (topological) and layout (physical) levels, as well as all the associated procedures for scripting its validation and optimization through transistor-level electrical simulations. This Python interface will be tested with three AMS soft-IP case studies in the field of high-resolution A/D data converters (ADCs), clock phase-locked loops (PLLs) and integrate-and-fire (IAF) modulators and their hard-IP implementation in a CMOS technology node ranging from 180nm to 22nm. All the above tasks will be performed in the IMB-CNM lab facilities at the UAB Bellaterra Campus.

How to apply

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- This offer can be found on: <u>https://www.imb-cnm.csic.es/en/about-center/careers/open-positions</u>
- More information on IMB-CNM: <u>https://www.imb-cnm.csic.es/en/</u>

