





Institute of Microelectronics of Barcelona IMB-CNM (CSIC) C/- dels Til·lers, S.N., Campus UAB | 08193, Cerdanyola del Vallès <u>https://www.imb-cnm.csic.es</u> | <u>rrhh@imb-cnm.csic.es</u> +34 93 594 7700

Job title

TFM: Low-Power Readout Circuits for

Smart Microelectronic Noses

Job description

Master Thesis

Descripction

Chemical sensors have been widely used in "electronic noses" for the analysis of volatile organic compounds. Employing chemical gas sensor arrays with pattern recognition in these devices allows boosting selectivity and reversibility for applications such as industrial process control, healthcare, and environmental monitoring.

In this project, you will investigate new bioinspired, low-power readout microcircuits for artificial olfaction using chemical gas microsensors fabricated at the clean room of the Institute of Microelectronics of Barcelona, IMB-CNM(CSIC). Your integrated circuit (IC) designs will be targeted to enable always-on operation, and efficient posterior artificial intelligence (AI) computing on portable devices powered by batteries or local energy harvesting. To this end, you will collaborate with a multidisciplinary team with expertise in neuroscience, computer science, chemistry and microelectronics.

Ideally, this Master Thesis should be the first step towards PhD studies dealing with smart low-power ROICs to improve performances and edge computing capabilities for IoT sensors.

Background and Skills

- Finishing a Master's degree in Electronics/IT Engineering (or similar) covering analog and digital VLSI circuit design, sensors and instrumentation, and signal processing.
- Competence with Cadence EDA tools for IC design.
- Experience programming in Python.
- Good spoken and written English
- Capability of working as a team.

Tasks

You will integrate circuit proposals for analog frontend, asynchronous A/D conversion, and digital communication stages in sub-micron CMOS technologies following the methodology described below:

- Functional modeling of the readout architecture in Python.
- Electrical modeling in Cadence Virtuoso using the Verilog-A language.







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 Mixed-signal circuit design and simulation at schematic and physical (layout) levels in Cadence Virtuoso, using hardware description languages such as VHDL for the digital synthesis.

How to apply

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- This offer can be found on: <u>https://www.imb-cnm.csic.es/en/about-center/careers/open-positions</u>
- More information on IMB-CNM: <u>https://www.imb-cnm.csic.es/en/</u>

