Project Type: **PhD Thesis**

**Implantable Area Networks for Massive μECoGs**

**Short Description**

The ICAS group of the IMB-CNMC is investigating a new generation of CMOS read-out integrated circuits (ROICs) for massive micro-electrocorticography (μECoG) of the brain. An implantable network of several ROICs is envisioned, being each ROIC capable of recording neural activity from a 1024-channel array of graphene transistors (GFETs). The core of this implantable area network is an application-specific integrated circuit (ASIC) in charge of both supplying the power to the ROICs and routing their digital communications through the contactless link with the external unit. This bridge ASIC may also contain some specific digital signal processing (DSP) for compressing the μECoG data to be transmitted due to the limited transcutaneous signal bandwidth available. Special attention will be paid to the low-power operation of this ASIC.

**Background & skills required**

- Electronic or Telecommunications Engineering (or any similar curriculum) covering the following topics: analog and digital CMOS circuit design and digital signal processing.
- Knowledge of EDA tools and languages for full-custom digital and mixed-signal ASIC design.
- Capability of working as a team.
- Good spoken and written English.

**Tasks**

Apart from the research work itself, the student will validate all circuit proposals through the design of the corresponding test chips following the full-custom digital and mixed-signal ASIC methodology. Target CMOS technologies will range from 0.18-μm to 65-nm nodes. The final ASIC candidate will also require in-vivo experimental characterization.

**Contact**

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